AMENDMENTS TO THE CLAIMS:

1. (Previously Presented) A circuit comprising a first and a second circuit module and a synchronization module, the first and the second module being mutually asynchronous, and the first and the second module being coupled by the synchronization module, the synchronization module comprising:

a transfer register for storing data which is communicated between the two circuit modules,

a control circuit for controlling the register in response to a respective timing signal from the first and the second circuit module, the control circuit comprising a control chain for generating a control signal for the transfer register the control chain including at least:

a repeater for inducing changes in the value of the control signal wherein the repeater is operable with a single input, and

one edge sensitive element for delaying a change in the value of the control signal until a transition in a selected one of the timing signals is detected.

2. (Previously Presented) A circuit according to claim 1, further comprising a comparator for generating a difference signal upon detection of a difference between an input and an output of the transfer register the control chain further comprising a wait element for delaying an active transition in the control signal until a difference is detected.

3. (Previously Presented) A circuit according to claim 1 wherein the control chain further comprises an arbitration element the arbitration element having respective channels for guiding at least a first and a second signal flow, the arbitration element being arranged for arbitrating between passing active events in the first and the second signal flow, the first channel being arranged between an output of the edge sensitive element and an input of the repeater.

4. (Previously Presented) A circuit according to claim 3, wherein the selected timing signal is a clock signal from the first circuit module wherein the timing signal from the second circuit module is an access request signal, the second channel of the arbitration element having a first input for receiving the access request signal and a first output for providing an access acknowledge signal to the second circuit module.

5. (Previously Presented) A circuit according to claim 3, further comprising an auxiliary register for transferring data from the first module to the register wherein the selected timing signal is a clock signal from the second circuit module wherein the timing signal from the first circuit module is a write request signal, the second channel of the arbitration element having a second input for receiving the write request signal and a second output for providing a control signal to control the auxiliary register.

6. (Previously Presented) A circuit according to claim 1 wherein the selected one of the timing signals is a clock signal from the first circuit module the circuit including an auxiliary register for transferring data from the transfer register to the second circuit module and wherein the circuit includes a further edge sensitive element for delaying a change in a control signal for the auxiliary register until a transition is detected in a timing signal from the second circuit module.

7. (Previously Presented) A circuit according to claim 6, wherein the further edge sensitive element is part of the control chain.

8. (Previously Presented) A circuit according to claim 6, wherein the further edge sensitive element is part of a further control chain, which is coupled to the control chain.

9. (Previously Presented) A circuit according to claim 1, wherein the synchronization module has a first transfer register for transferring data from the first to the second circuit module and a second transfer register for transferring data from the second to the first circuit module the transfer registers being controlled by the same control signal.

10. (Previously Presented) A method for transferring data between a first and a second circuit module using a synchronization module the first and the second module being mutually asynchronous, and the first and the second module being coupled by the synchronization module, the method comprising:

temporarily storing data which is transferred from the first to the second circuit module in a register,

controlling the register in response to a respective timing signal from the first, and the second circuit module, by a control circuit which comprises a control chain for generating a control signal wherein:

changes are induced in the value of the control signal,

a change in the control signal value is delayed until a transition in a selected one of the timing signals is detected and

wherein the changes are operable to be induced through a single input.

11. (Previously Presented) A method according to claim 10, wherein the changes are introduced through a repeater.

12. (Previously Presented) A method according to claim 10, further comprising a edge sensitive element to delaying the change in the control signal value.

13. (Previously Presented) A method according to claim 12 wherein the selected one of the timing signals is a clock signal from the first module the circuit including an auxiliary register for transferring data from the transfer register to the second circuit module.

14. (Previously Presented) A method according to claim 13, wherein the circuit includes a further edge sensitive element for delaying a change in a control signal for the auxiliary register until a transition is detected in a timing signal from the second circuit module.

15. (Previously Presented) A method according to claim 14, wherein the further edge sensitive element is part of the control chain.

16. (Previously Presented) A method according to claim 14, wherein the further edge sensitive element is part of a further control chain, which is coupled to the control chain.

17. (Previously Presented) A method according to claim 13, wherein the control chain further comprises an arbitration element the arbitration element having respective channels for guiding at least a first and a second signal flow, the arbitration element being arranged for arbitrating between passing active events in the first and the second signal flow, the first channel being arranged between an output of the edge sensitive element and an input of the repeater.

18. (Previously Presented) A synchronization module, comprising:

a first and a second circuit module and a synchronization module, the first and the second circuit module being mutually asynchronous, and the first and the second circuit module being coupled by the synchronization module,

a transfer register for storing data which is communicated between the two circuit modules,

a control circuit for controlling the register in response to a respective timing signal from the first and the second circuit module, the control circuit comprising a control chain for generating a control signal for the transfer register, wherein the control chain comprises a single input that is fed into a repeater for inducing changes in the value of the control signal; and one edge sensitive element for delaying a change in the signal value until a transition in a selected one of the timing signals is detected.

19. (Previously Presented) A module according to claim 18, further comprising a comparator for generating a difference signal upon detection of a difference between an input and an output of the transfer register the control chain further comprising a wait element for delaying an active transition in the control signal until a difference is detected.

20. (Previously Presented) A module according to claim 18, wherein the control chain further comprises an arbitration element the arbitration element having respective channels for guiding at least a first and a second signal flow, the arbitration element being arranged for arbitrating between passing active events in the first and the second signal flow, the first channel being arranged between an output of the edge sensitive element and an input of the repeater.